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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/043,223 | 01/14/2002 | Gil Vinitzky | 1102-US | 6216 |

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| EXAMINER | |
|---|---|
| BUEHL, BRETT J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/043,223 | VINITZKY, GIL | |
| | Examiner | Art Unit | |
| | Brett J Buehl | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-11 have been examined.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration and Fees as received on 1/14/02.

### *Specification*

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 7-11 recites the limitation "said...steps" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 1 should be amended to read, "the method comprising the steps of".

8. Claim 10 states the limitation, "wherein any of said steps are applied to a given processor configuration a plurality of times for a plurality of different values of n". Use of the variable 'n' renders this claim indefinite since it can be taken to mean a negative value, zero or infinity. These values, when applied to the number of phases in a pipeline processor, present situations that cannot occur. Please amend the claim language to more clearly define the metes and bounds of the claimed invention. Similar corrections are also required for claim 11.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3 and 7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lauterbach.

11. Regarding claim 1, Lauterbach has taught a method of converting a computer processor configuration having a k-phased pipeline into a virtual multithreaded processor, the method comprising:

a. Dividing each pipeline phase of said processor configuration into a plurality n of sub-phases (Figure 2 and Paragraph 32); and

b. Creating at least one virtual pipeline within said pipeline, said virtual pipeline comprising k sub-phases. Since the virtual pipeline is not a physical entity, any k sub-stages of Lauterbach form a virtual pipeline.

12. Regarding claim 2, Lauterbach has taught a method according to claim 1 and further comprising executing a different thread within each one of said virtual pipelines (Paragraph 32, 2nd sentence).

13. Regarding claim 3, Lauterbach has taught a method according to claim 2 wherein said executing step comprises executing any of said threads at an effective clock rate equal to the clock rate of said k-phased pipeline. Since Lauterbach has sub-divided the stages into a number of sub-stages equal to the number of threads, the clock rate would have increased by a multiple of that number, thereby executing the threads at an effective rate equal to the non-divided processor.

14. Regarding claim 7, Lauterbach has taught a method according to claim 1 wherein any of said steps are applied to a single-threaded processor configuration (Figures 1 & 2).

15. Regarding claim 8, Lauterbach has taught a method according to claim 1 wherein any of said steps are applied to a multithreaded processor configuration. (Figure 2 and Paragraph 32).

16. Regarding claim 9, Lauterbach has taught a method according to claim 1 wherein any of said steps are applied to a given processor configuration a plurality of times for a plurality of different values of n, thereby creating a plurality of different processor configurations (Paragraph 32).

17. Regarding claim 10, Lauterbach has taught a method according to claim 1 wherein any of said steps are applied to a given processor configuration a plurality of times for a plurality of

different values of n (Figure 2 and Paragraph 32) until a target processor performance level is achieved. Applying the steps a plurality of times would merely deepen the pipeline by several phases at a time, basically achieving the same goal as if applying the steps once with n being equal to the aggregate number of phases, which is disclosed by Lauterbach. As for the performance level, Lauterbach's predefined target performance level is the number threads desired to run on the processor, and the value of n is the number of threads, thus the number of times the stages are sub-divided.

18. Regarding claim 11, Lauterbach has taught a method according to claim 1 wherein said dividing step comprises: selecting a predefined target processor performance value; and selecting a value of n being in predefined association with said predefined target processor performance level. Lauterbach's predefined target performance level is the number threads desired to run on the processor, and the value of n is the number of threads, thus the number of times the stages are sub-divided.

***Claim Rejections - 35 USC § 103***

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lauterbach as applied to claim 1 above, and further in view of Hennessy.

21. Regarding claim 4, Lauterbach discloses the invention substantially as claimed. However, Lauterbach does not disclose the manner in which the stages are sub-divided.

22. Hennessy teaches superpipelining a pipeline processor by increasing the number of pipeline stages and rebalancing the sub-stages (page 510, 3rd paragraph). Rebalancing the sub-stages refers to the operation of evenly distributing the workload, and thus the cycle time, between the sub-stages.

23. Accordingly, it was well known in the art at the time of the invention that increasing the number of stages in a pipeline by sub-dividing existing stages requires determining a minimum cycle time and distributing the cycle time evenly amongst the sub-stages. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Hennessy to determine the delay and to balance the delay between the sub-stages of Lauterbach for the desirable purpose of increasing the clock speed, thereby also increasing the pipeline throughput.

24. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lauterbach as applied to claims 1 and 2 above, and further in view of Culler.

25. Regarding claim 5, Lauterbach discloses the invention substantially as claimed. However, Lauterbach does not disclose replicating the register set.

26. Culler teaches an interleaved multithreading scheme that utilized replicated register sets, one for each of the threads, in order for the threads to function independently without register conflicts.

27. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Culler in the invention of Lauterbach and

provide replicated register sets so that the independent threads run without encountering register conflicts between threads, since register conflicts degrade performance. The advantages of replicating the register sets as taught by Culler provides sufficient suggestion and motivation to one of ordinary skill in the art to follow the teachings of Culler and modify the invention of Lauterbach to allow each thread its own register set.

28. Regarding claim 6, Lauterbach and Culler have taught a method according to claim 5 and further comprising: selecting any of said threads at a clock cycle; and activating at said clock cycle the register set that is associated with said selected thread. Selecting a thread is the basic idea behind interleaved multithreading, as disclosed by Lauterbach and Culler. As for the register sets, Culler discloses a multithreaded pipelined processor with replicated register sets, one for each thread (Culler: Page 905, The Basic Interleaved Scheme). In order for the registers of a given thread to be accessible when the corresponding thread is activated, the corresponding register set would also have been activated.

***Conclusion***

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of art disclosed by the references cited and the objections made. Applicant must show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

30. Goossens has taught a super-pipelined, superscalar computer processor implementing a cycle-by-cycle interleaving scheme. The processor has replicated register sets, one for each of the four threads, and a faster clock due to the deeper pipeline.

31. Parady has taught a multithreaded processor with four threads. He indicates that other numbers of threads are possible, but more than four threads results in a loss of performance (col. 4, lines 9-18).

32. Inquiries concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl who can be reached at (703) 305-4663 or <brett.buehl@uspto.gov>. The examiner can normally be reached between the hours 8:00am – 5:30pm (EST), Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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